CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for controlling resistance variation in a variable resistance memory device, the method comprising:

a) categorizing a variable resistance memory cell as being in either an "on" state or an "off" state based on a resistance level of the memory cell;

b) if the memory cell is categorized as being in the "on" state, determining if the resistance level of the memory cell is outside a predetermined resistance range for the "on" state;

c) if the memory cell is categorized as being in the off state, determining if the resistance level of the memory cell is outside a predetermined resistance range for the "off" state;

d) applying a reset pulse to the memory cell to restore an original resistance profile of the memory cell if the condition tested for in either b) or c) is determined to exist in the memory cell.

2. The method according to claim 1, wherein determining if the resistance level of the memory cell is outside a predetermined resistance range for the "on" state includes determining if the resistance level of the memory cell is greater than a predetermined maximum resistance level for the "on" state.

3. The method according to claim 2, wherein the reset pulse applied to the memory cell is a "hard" write pulse for restoring an original resistance level for the "on" state if the resistance level of the memory cell is greater than the predetermined maximum.

4. The method according to claim 3, wherein the "hard" write pulse is in the form of a pulse having at least one of a voltage magnitude greater than a predetermined threshold voltage level of a normal write signal and a pulse width greater than that of a predetermined pulse width of a normal write signal.

5. The method according to claim 2, wherein the reset pulse applied to the memory cell is at least one "soft" write pulse for restoring an original resistance level for the "on" state if the resistance level of the memory cell is greater than the predetermined maximum.

6. The method according to claim 5, wherein the "soft" write pulse is in the form of a pulse having at least one of a voltage magnitude less than a predetermined threshold voltage level of a normal write signal and a pulse width less than that of a predetermined pulse width of a normal write signal.

7. The method according to claim 1, wherein determining if the resistance level of the memory cell is outside a predetermined resistance range for the "on" state includes determining if the resistance level of the memory cell is less than a predetermined minimum resistance level for the "on" state.

8. The method according to claim 7, wherein the reset pulse applied to the memory cell is at least one "soft" erase pulse for restoring an original resistance level for the "on" state if the resistance level of the memory cell is less than the predetermined minimum.

9. The method according to claim 8, wherein the "soft" write erase pulse is in the form of a pulse having at least one of a voltage magnitude less than a predetermined threshold voltage level of a normal erase signal and a pulse width less than that of a predetermined pulse width of a normal erase signal.

10. The method according to claim 1, wherein determining if the resistance level of the memory cell is outside a predetermined resistance range for the "off" state includes determining if the resistance level of the memory cell is less than a predetermined minimum resistance level for the "off" state.

11. The method according to claim 10, wherein the reset pulse applied to the memory cell is a "hard" erase pulse for restoring an original resistance level for the

"off" state if the resistance level of the memory cell is less than the predetermined minimum.

12. The method according to claim 11, wherein the "hard" erase pulse is in the form of a pulse having at least one of a voltage magnitude greater than a predetermined threshold voltage level of a normal erase signal and a pulse width greater than that of a predetermined pulse width of a normal erase signal.

13. The method according to claim 10, wherein the reset pulse applied to the memory cell is at least one "soft" erase pulse for restoring an original resistance level for the "off" state if the resistance level of the memory cell is less than the predetermined minimum.

14. The method according to claim 13, wherein the "soft" write erase pulse is in the form of a pulse having at least one of a voltage magnitude less than a predetermined threshold voltage level of a normal erase signal and a pulse width less than that of a predetermined pulse width of a normal erase signal.

15. The method according to claim 1, wherein determining if the resistance level of the memory cell is outside a predetermined resistance range for the "off" state

includes determining if the resistance level of the memory cell is greater than a predetermined maximum resistance level for the "off" state.

16. The method according to claim 15, wherein the reset pulse applied to the memory cell is at least one "soft" write pulse for restoring an original resistance level for the "off" state if the resistance level of the memory cell is greater than the predetermined maximum.

17. The method according to claim 16, wherein the "soft" write pulse is in the form of a pulse having at least one of a voltage magnitude less than a predetermined threshold voltage level of a normal write signal and a pulse width less than that of a predetermined pulse width of a normal write signal.

18. The method according to claim 1, wherein acts a) through d) are performed at a predetermined frequency during operation of a processor device.

19. The method according to claim 1, wherein the memory cell is a PCRAM cell.

20. The method according to claim 19, wherein the PCRAM cell includes a silver selenide layer.

21. The method according to claim 1, further comprising:

e) prior to categorizing the variable resistance memory cell, selecting the memory cell from among an array of variable resistance memory cells; and

f) repeating e) and a) through d) for another memory cell within the array of memory cells.

22. The method according to claim 21, further comprising performing a plurality of write/erase cycles in the array of variable resistance memory cells during operation of a processor device, and wherein the acts of e), a) through d) and f) are performed together at a predetermined frequency during the operation of a processor device.

23. A method for controlling a drift condition towards an overly low resistance in a high resistance state in a variable resistance memory cell, comprising:

a) comparing the resistance level of the memory cell with a reference level and identifying the memory cell as being in a high resistance state if the resistance level is above the reference level;

b) if the memory cell is identified as being in the high resistance state, comparing the resistance level of the memory cell with a predetermined minimum resistance level;

c) if the resistance level of the memory cell is not greater than the predetermined minimum resistance level, applying a reset pulse to the memory cell to restore an original resistance level for the high resistance state of the memory cell.

24. The method according to claim 23, wherein the reset pulse is a "hard" reset pulse applied in a direction to raise the resistance level in the high resistance state above the predetermined minimum resistance level.

25. The method according to claim 23, wherein the reset pulse is at least one "soft" reset pulse applied in a direction to raise the resistance level in the high resistance state above the predetermined minimum resistance level.

26. The method according to claim 23, wherein the memory cell is a PCRAM cell.

27. The method according to claim 24, wherein the PCRAM cell includes a silver selenide layer.

28. A method for controlling a drift condition towards an overly high resistance in a low resistance state in a variable resistance memory cell, comprising:

a) comparing a resistance level of the memory cell with a reference level and identifying the memory cell as being in a low resistance state if the resistance level is below the reference level;

b) if the memory cell is identified as being in the low resistance state, comparing the resistance level of the memory cell with a predetermined maximum resistance level;

c) if the resistance level of the memory cell is not less than the predetermined maximum resistance level, applying a reset pulse to the memory cell to restore an original resistance level for the low resistance state of the memory cell.

29. The method according to claim 28, wherein the reset pulse is a "hard" reset pulse applied in a direction to lower the resistance level in the low resistance state below the predetermined maximum resistance level.

30. The method according to claim 28, wherein the reset pulse is at least one "soft" reset pulse applied in a direction to lower the resistance level in the low resistance state below the predetermined maximum resistance level.

31. The method according to claim 28, wherein the memory cell is a PCRAM cell.

32. The method according to claim 31, wherein the PCRAM cell includes a silver selenide layer.

33. A method for controlling a drift condition towards an excessively high resistance in a high resistance state in a variable resistance memory cell, comprising:

a) comparing the resistance level of the memory cell with a reference level and identifying the memory cell as being in a high resistance state if the resistance level is above the reference level;

b) if the memory cell is identified as being in the high resistance state, comparing the resistance level of the memory cell with a predetermined maximum resistance level;

c) if the resistance level of the memory cell is not less than the predetermined maximum resistance level, applying a reset pulse to the memory cell to restore an original resistance level for the high resistance state of the memory cell.

34. The method according to claim 33, wherein the reset pulse is a "hard" reset pulse applied in a direction to lower the resistance level in the high resistance state below the predetermined maximum resistance level.

35. The method according to claim 33, wherein the reset pulse is at least one "soft" reset pulse applied in a direction to lower the resistance level in the high resistance state below the predetermined maximum resistance level.

36. The method according to claim 33, wherein the memory cell is a PCRAM cell.

37. The method according to claim 36, wherein the PCRAM cell includes a silver selenide layer.

38. A method for controlling a drift condition towards an excessively low resistance in a low resistance state in a variable resistance memory cell, comprising:

a) comparing a resistance level of the memory cell with a reference level and identifying the memory cell as being in a low resistance state if the resistance level is below the reference level;

b) if the memory cell is identified as being in the low resistance state, comparing the resistance level of the memory cell with a predetermined minimum resistance level;

c) if the resistance level of the memory cell is not greater than the predetermined minimum resistance level, applying a reset pulse to the memory cell to restore an original resistance level for the low resistance state of the memory cell.

39. The method according to claim 38, wherein the reset pulse is a "hard" reset pulse applied in a direction to raise the resistance level in the low resistance state above the predetermined minimum resistance level.

40. The method according to claim 38, wherein the reset pulse is at least one "soft" reset pulse applied in a direction to raise the resistance level in the low resistance state above the predetermined minimum resistance level.

41. The method according to claim 38, wherein the memory cell is a PCRAM cell.

42. The method according to claim 41, wherein the PCRAM cell includes a silver selenide layer.

43. A method for operating a PCRAM memory device including an array of variable resistance memory cells, comprising:

determining that a resistance level of a PCRAM memory cell in a high resistance state has deviated from an initial resistance level for a high resistance state thereof; and

applying at least one voltage potential to the memory cell to restore the initial resistance level for the high resistance state.

44. The method according to claim 43, wherein the at least one voltage potential applied is a "hard" erase pulse.

45. The method according to claim 43, wherein the at least one voltage potential applied is at least one "soft" erase pulse.

46. The method according to claim 43, wherein the at least one voltage potential applied is at least one "soft" write pulse.

47. The method according to claim 43, wherein the voltage potential is applied when the resistance level of the PCRAM memory cell is determined to have deviated from the initial resistance level by an amount beyond a predetermined limit.

48. A method for operating a PCRAM memory device including an array of variable resistance memory cells, comprising:

determining that a resistance level of a PCRAM memory cell in a low resistance state has deviated from an initial resistance level for a low resistance state thereof; and

applying at least one voltage potential to the memory cell to restore the initial resistance level for the low resistance state.

49. The method according to claim 48, wherein the at least one voltage potential applied is a "hard" write pulse.

50. The method according to claim 48, wherein the at least one voltage potential applied is at least on "soft" write pulse.

51. The method according to claim 48, wherein the at least one voltage potential applied is at least on "soft" erase pulse.

52. The method according to claim 48, wherein the voltage potential is applied when the resistance level of the PCRAM memory cell is determined to have deviated from the initial resistance level by an amount beyond a predetermined limit.

53. A method for operating a PCRAM memory device including an array of variable resistance memory cells, comprising:

determining that a resistance profile of a PCRAM memory cell has deviated from an initial resistance profile of the memory cell; and

applying at least one voltage potential to the memory cell to restore the initial resistance profile for the memory cell.

54. A method for operating a PCRAM memory device including an array of variable resistance memory cells, comprising:

categorizing a variable resistance memory cell as being in either an "on" state or an "off" state based on a current resistance level of the memory cell; and

applying at least one reset pulse to the memory cell to restore the initial resistance profile for the memory cell based on the "on" or "off" state of the cell and a direction of the resistance profile to be restored relative to the current resistance level of the memory cell.

55. The method according to claim 54, wherein the at least one reset pulse applied is a "hard" write pulse.

56. The method according to claim 54, wherein the at least one reset pulse applied is a "hard" erase pulse.

57. The method according to claim 54, wherein the at least on reset pulse applied is at least one "soft" write pulse.

58. The method according to claim 54, wherein the at least on reset pulse applied is at least one "soft" erase pulse.

59. A memory device comprising:

an array of variable resistance memory cells; and

a controller coupled to the memory array and which periodically performs an algorithm to detect resistance profile drift in the memory cells of the array, and which restores an original resistance profile in any memory cells in which resistance profile drift is detected.

60. The memory device according to claim 59, wherein the controller controls application of a "hard" write pulse to a memory cell in the array if the controller detects that a resistance level of the memory cell is in a low resistance state and has deviated from an original resistance level for the low resistance state to an underwrite condition.

61. The memory device according to claim 59, wherein the controller controls application of at least one "soft" write pulse to a memory cell in the array if the controller detects that a resistance level of the memory cell is in a low resistance state and has deviated from an original resistance level for the low resistance state to an underwrite condition.

62. The memory device according to claim 59, wherein the controller controls application of a "soft" erase pulse to a memory cell in the array if the controller detects that a resistance level of the memory cell is in a low resistance state and has deviated from an original resistance level for the low resistance state to an overwrite condition.

63. The memory device according to claim 59, wherein the controller controls application of a "hard" erase pulse to any memory cell in the array if the controller detects that a resistance level of the memory cell is in a high resistance state and has deviated from an original resistance level for the high resistance state to an undererase condition.

64. The memory device according to claim 59, wherein the controller controls application of a "soft" erase pulse to a memory cell in the array if the controller detects that a resistance level of the memory cell is in a high resistance state and has deviated from an original resistance level for the high resistance state to an undererase condition.

65. The memory device according to claim 59, wherein the controller controls application of a "soft" write pulse to a memory cell in the array if the controller detects that a resistance level of the memory cell is in a high resistance state and has deviated from an original resistance level for the high resistance state to an overerase condition.

66. A processor system, comprising:

a processor for receiving and processing data;

at least one memory array of variable resistance memory cells for exchanging data with the processor; and

a controller connected to the at least one memory array, wherein the controller

manages memory access requests from the processor to the at least one memory device,

periodically performs an algorithm to detect resistance profile drift in the memory cells of the array, and

restores an original resistance profile in any memory cells in which resistance profile drift is detected.

67. A processor system, comprising:

a processor for receiving and processing data;

at least one memory array of variable resistance memory cells for exchanging data with the processor; and

a controller connected to the at least one memory array, wherein the controller performs an algorithm which

detects if the resistance of any of the memory cells among the array is in a high resistance state, and whether the resistance of any cells detected to be in the

high resistance cells is below a predetermined minimum level or is above a predetermined maximum level for the high resistance state,

controls application of at least one reset pulse to any cells detected to be in the high resistance state and having a resistance either below the predetermined minimum level or above the predetermined maximum level to thereby restore a predetermined resistance range for the high resistance state,

detects if the resistance of any of the memory cells among the array is in a low resistance state, and whether the resistance of any cells detected to be in the low resistance state is above a predetermined maximum level or is below a predetermined minimum level for the low resistance state, and

controls application of at least one reset pulse to any cells detected to be in the low resistance state and having a resistance either above the predetermined maximum level or below the predetermined minimum level to thereby restore a predetermined resistance range for the low resistance state.

68. The processor system according to claim 67, wherein the controller performs the algorithm at predetermined time intervals.